REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-3 and 5-13 remain in the application and are subject to examination. Claim 1 has been amended. No claims have been added or canceled herein. Claim 4 was previously canceled.

In "Claim Objections" on page 2 of the above-identified Office Action, the Examiner objected to claim 1 because of an informality. The objectionable phrase has been deleted.

In "Claim Rejections - 35 USC § 103" on pages 2-7 of the Office Action, claims 1-3 and 5-13 have been rejected as being obvious over U.S. Patent No. 5,455,453 to Harada et al. (hereinafter Harada) in view of U.S. Patent No. 5,646,434 to Chrysostomides (hereinafter Chrysostomides) and U.S. Patent No. 5,416,660 to Shiga under 35 U.S.C. § 103(a).

In "Claim Rejections - 35 USC § 103" on pages 7-12 of the Office Action, claims 1-3 and 5-13 have also been rejected as being obvious over U.S. Patent No. 6,476,486 to Humphrey et al. (hereinafter Humphrey) in view of Chrysostomides and Shiga under 35 U.S.C. § 103(a).

As will be explained below, it is believed that the claims were patentable over the cited art in their previous form and, therefore, the claims have not been amended to overcome the references.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, a semiconductor component comprising:

> a semiconductor chip including an electronic circuit configured in said semiconductor chip, said electronic circuit having a terminal for a signal to be processed, a stage connected to said terminal for the signal, a terminal for obtaining a supply potential, said terminal for obtaining the supply potential being connected to said stage, said stage being selected from a group consisting of an input stage and an output stage;
>
> a first conductor track running outside said semiconductor chip, said first conductor track being connected to said terminal for the signal;
>
> a second conductor track running outside said semiconductor chip, said second conductor track being connected to said terminal for obtaining the supply potential;
>
> a further conductor track running outside said semiconductor chip, said further conductor track being connected to said second conductor track, said further conductor track entirely surrounding said semiconductor chip, said further conductor track crossing said first conductor track, defining a crossing location, and said further conductor track crossing said second conductor track; and
>
> an electrostatic discharge protection element for carrying an electrostatic discharge away from said terminal for the signal and to the supply potential, said electrostatic discharge protection element being

> disposed outside of said semiconductor chip, said electrostatic discharge protection element being connected outside of said semiconductor chip to said further conductor track and to said first conductor track, said electrostatic discharge protection element being disposed close to said crossing location.

Thus, claim 1 calls for an electrostatic discharge protection element being connected to a further conductor track connected to a second conductor track connected to a terminal for obtaining a supply potential, and the electrostatic discharge protection element being connected to a first conductor track connected to a terminal for a signal.

Therefore, in claim 1, the electrostatic discharge protection element is connected to a conductor track associated with a signal and a conductor track associated with a supply potential.

The Harada reference discloses a semiconductor element or integrated circuit 8 which is disposed on an insulating film or substrate 2. The substrate 2 carries a wiring or supply line 3 for the VCC voltage and a wiring or supply line 4 for the ground voltage GND. Signals are supplied through wirings or lines 5. There is no hint or suggestion in Harada of connecting an electrostatic discharge element between a conductor track associated with a signal and a conductor track associated with a supply potential.

It appears to be an object of Harada to minimize discrete components on the substrate film 2. For example, film resistors 10 are disposed in the conductor tracks 5 for the signals themselves (see column 8, lines 24 - 25) so that resistors 10 probably function as matching resistors rather than ESD protection elements.

As mentioned above, the invention of the instant application as claimed calls for a first conductor track being connected to a terminal for the signal, a further conductor track being connected to the second conductor track which, in turn, is connected to a supply potential, wherein the electrostatic discharge protection element is connected to the further conductor track and the first conductor track.

In contrast, the resistors of Harada are not connected to a supply potential line, e.g., the wiring or conductor track 4 for the ground voltage or the wiring or conductor track 3 for the VCC voltage.

The Chrysostomides reference has all of its electrostatic discharge elements on-chip and not outside the chip. The Shiga reference fails to disclose how to connect the ESD element 2 to a supply potential track.

The Examiner has also applied Humphrey in combination with Chrysostomides and Shiga against the claims. Humphrey discloses a power supply ring 17 and a ground voltage ring 15, both surrounding an integrated circuit chip 20. The Examiner refers to diode Z3. However, the diode Z3 is connected between the power and ground supply lines 17, 15. See the lower-left corner of Fig. 8 of Humphrey. This means that the diode Z3 is an element for stabilizing the supply voltage VSS, GND rather than an ESD protection element which is used to drain excess overvoltage resulting from an ESD event from a signal terminal to a power or ground terminal of the chip. Since the diode Z3 is connected at both of its terminals to power supply lines, a person skilled in the art would not attempt to connect the diode Z3 otherwise, since that would establish a different function for the diode Z3.

As explained above, the Chrysostomides and Shiga references are also not suited to teach a skilled person to modify Humphrey to render the present invention obvious.

Clearly, neither Harada nor Humphrey in combination with Chrysostomides and Shiga show or suggest an electrostatic discharge protection element connected to a conductor track associated with a signal and a conductor track associated

with a supply potential, as recited in claim 1 of the instant application.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1.

In view of the foregoing, reconsideration and allowance of claims 1-3 and 5-13 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time is required, petition for extension is herewith made. Any extension fee associated therewith should be charged to Deposit Account Number 12-1099 of Lerner Greenberg Stemer LLP.

Appl. No. 10/623,815
Amdt. dated 7/12/06
Reply to Office action of 4/14/06

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to Deposit Account Number 12-1099 of Lerner Greenberg Stemer LLP.

Respectfully submitted,

Laurence A. Greenberg (29,308)

LAG/bb

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Lerner Greenberg Stemer LLP
P.O. Box 2480
Hollywood, Florida 33022-2480
Tel.: (954) 925-1100
Fax: (954) 925-1101